LOADLESS NMOS FOUR TRANSISTOR DYNAMIC DUAL VT SRAM CELL

Abstract of the Disclosure

Loadless 4T SRAM cells, and methods for operating such SRAM cells, which can provide highly integrated semiconductor memory devices while providing increased performance with respect to data stability and increased I/O speed for data access operations. A loadless 4T SRAM cell comprises a pair of access transistors and a pair of pull-down transistors, all of which are implemented as N-channel transistors (NFETs or NMOSFETS). The access transistors have lower threshold voltages than the pull-down transistors, which enables the SRAM cell to effectively maintain a logic "1" potential during standby. The pull-down transistors have larger channel widths as compared to the access transistors, which enables the SRAM cell to effectively maintain a logic "0" potential at a given storage node during a read operation. A method is implemented for dynamically adjusting the threshold voltages of the transistors of activated memory cells during an access operation to thereby increase the read current or performance of the accessed memory cells.